

ABSTRACT

A reconfigurable processor for processing digital logic functions includes a microcontroller, one or more decoders connected to the microcontroller, a plurality of interconnection busses; and a plurality of processing elements is described. Each processing element connects to one or more other processing elements by local interconnection paths and to a decoder. The plurality of processing elements are arranged in one or more pipeline stages each including one or more processing elements. A method of dynamically reconfiguring a pipelined processor including configuring, using a microcontroller, a plurality of pipeline stages each including one or more processing elements, processing data through one or more pipeline stages, reconfiguring, by the microcontroller, one or more pipeline stages to define one or more subsequent pipeline stages, and routing the processed data through the one or more reconfigured pipeline stages is also described. The reconfiguration may take place while data is processed by other pipeline stages.